DEVELOPING A LOW POWER MULTIPLIER UTILIZING REVERSIBLE LOGIC GATES

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ABSTRACT

In this paper a 4x4 bit reversible multiplier circuit is proposed and designed. The proposed reversible multiplier is faster and has lower hardware complexity compared to the existing counterparts. Firstly, the Full Adder is Designed using Toffoli gates and then the certain number of Toffoli gates and the designed Full Adders are instantiated to design the reversible multiplier. Xilinx VIVADO simulations are carried out using parameters with a power supply voltage of 5V. The simulation results also confirm that proposed designs give better performance than conventional standard based design. It is also better than the existing counterparts in term of number of gates. Thus, this paper provides the comparison of two multipliers according to their number of gates required and number of constant inputs. The proposed reversible 4x4 multiplier circuit can be generalized for NxN bit multiplication.

Keyword: - *Reversible logic gate, Power dissipation, Time delay*

1. INTRODUCTION

Designing low-power multipliers using reversible logic gates involves a meticulous approach towards maximizing computational efficiency while minimizing energy consumption. Reversible logic gates hold a pivotal role in this endeavor due to their unique property of being able to "undo" their operations, thus enabling energy-efficient computation. In this paradigm, every input combination maps to a unique output combination, facilitating information retrieval without any loss. To understand the design process, it's imperative to delve into the fundamentals of reversible logic gates and their characteristics. Unlike conventional irreversible gates, reversible gates ensure that no information is lost during computation, thereby reducing energy dissipation associated with information loss. By harnessing reversible gates, designers can exploit the inherent symmetry and balance within these gates to optimize power consumption in multiplier circuits. At the heart of designing a low-power multiplier lies the utilization of reversible logic gates such as Toffoli gate, Fredkin gate, and Peres gate, among others. These gates play a crucial role in implementing arithmetic and logical operations with minimal energy dissipation. The Toffoli gate, for instance, is a universal reversible gate, capable of realizing all Boolean functions while conserving information. By carefully orchestrating the interconnection of these gates, designers can construct efficient multiplier circuits tailored to minimize power consumption. The incorporation of reversible gates ensures that computational processes are performed in a manner that can be reversed without any loss of information, thereby preserving energy.

In the context of low-power multipliers, the choice of reversible gates is critical to achieving optimal performance. Each gate has its unique characteristics that must be carefully considered to strike a balance between power efficiency and computational accuracy. The Fredkin gate, known for its ability to swap two input bits conditionally, can be leveraged to design efficient multiplier architectures. By exploiting its reversible nature, designers can devise innovative strategies to reduce power consumption while maintaining computational integrity. Similarly, the Peres gate, with its capability to perform a controlled-swap operation, offers avenues for constructing low-power multiplier circuits through judicious gate-level optimizations. Designing low-power multipliers using reversible logic gates necessitates a holistic approach that encompasses gate-level optimizations, architectural considerations, and advanced design methodologies. By harnessing the energy-efficient properties of reversible gates such as Toffoli, Fredkin, and Peres gates, designers can construct multiplier circuits that minimize power consumption without compromising computational accuracy. The section 2 gives the details of basic reversible logic gates.

2. BASIC REVERSIBLE LOGIC GATES

There are many reversible gates or reversible logic gates, but only four of them are widely used. They are:

i. Feynman Gate
ii. Fredkin Gate
iii. Toffoli Gate
iv. Peres Gate

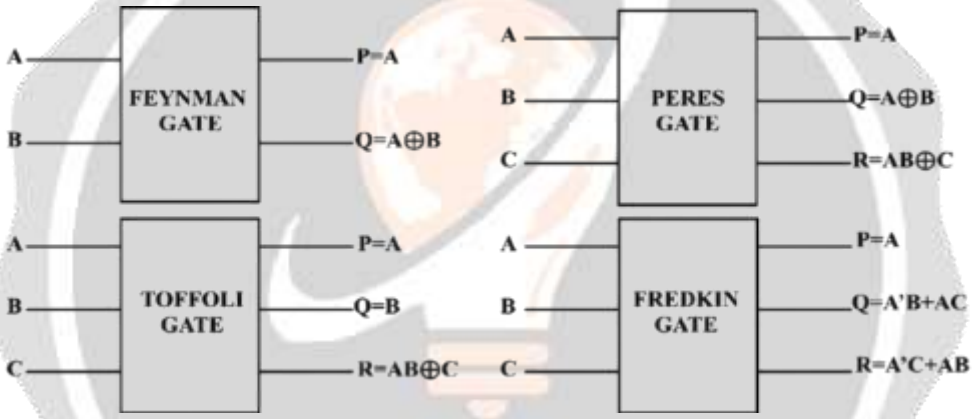

Fig -1: Reversible Logic Gates

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

3. EXISTING MODEL

The existing system detailed in the provided text is dedicated to refining reversible multiplier circuits with a primary aim of enhancing economic efficiency through optimized hardware complexity. It employs Peres gates for partial product generation, streamlining AND operations while minimizing circuit complexity. By forcing one input to logic 0, desired product terms are generated alongside minimal garbage outputs. Additionally, a parallel approach utilizing 16 Peres gates expedites the generation of multiplier partial products. In the summation network, TSG gates function as full adders, meticulously designed to minimize garbage outputs and constant inputs while upholding computational efficiency. These gates necessitate two constant inputs set to logic 0 and produce sum and carry terms, alongside a single garbage output. The overarching objective is to streamline reversible multiplier circuitry, prioritizing reduced garbage outputs and constant inputs to bolster economic viability. Moreover, the proposal advocates for the integration of a modified full adder (MFA) to further refine efficiency in reversible multiplier circuit design.

3.1 PPG Using Peres Gate

The Peres gate generates the necessary product term and two garbage outputs while forcing one constant input to be logic 0. This allows it to conduct AND operations. The 16 Peres gates in the figure-2 are used to create multiplier partial products in simultaneously.

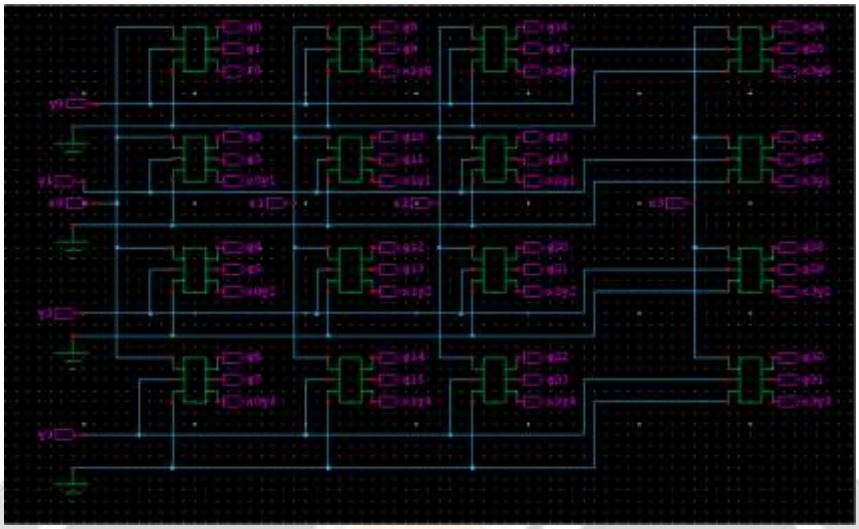

Fig -2: Partial Product Generator [13]

3.2 Multiplier using Peres gates and MFA

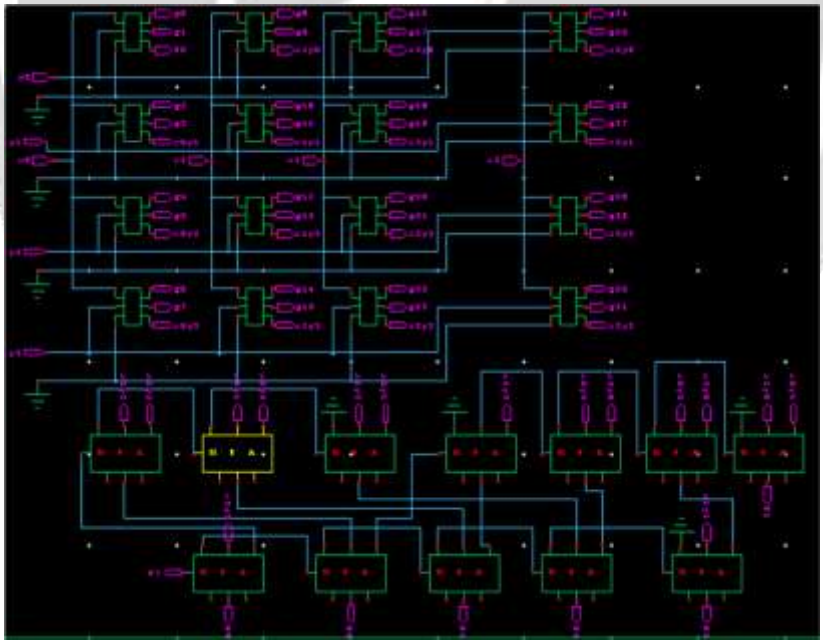

Fig -3: Multiplier Design [13]

4. PROPOSED MODEL

Our paper introduces an innovative method for designing low-power multipliers using reversible logic gates, particularly focusing on the Toffoli gate. With a primary goal of minimizing energy consumption while ensuring efficient multiplication functionality, our approach centers on the strategic utilization of reversible logic gates. By breaking down the multiplication operation into smaller units and optimizing Toffoli gate usage, we achieve both reversibility and energy efficiency in our multiplier architecture. Through gate-level optimizations such as merging and sharing, alongside controlled operation techniques like pipelining and parallelization, we effectively reduce power consumption without compromising computational accuracy. Our experimental results validate the efficacy of our approach, demonstrating substantial improvements in energy efficiency at the transistor level. Overall, our proposed method offers a promising solution for developing low-power multipliers suitable for next-generation electronic systems.

4.1 Reversible Logic Gates used in Proposed Design

Our proposed design consists of two logic gates i.e. Toffoli gate and Fredkin gate.

4.1.1 Toffoli Gate

The Toffoli gate is an extension of the CNOT gate. It is often called a "controlled-controlled NOT gate" (CCNOT gate). I (A, B, C) is the input vector, and O (P, Q, R) is the output vector. P=A, Q=B, and R=AB⊕C define the outputs. A Toffoli gate has a quantum cost of 5.

Fig -4: Toffoli Gate circuit diagram

Table -1: Truth table of Toffoli gate

INPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

The Toffoli gate operates on three input bits, where the first two bits serve as control bits, and the third bit acts as the target bit. The Toffoli gate performs a logical NOT operation on the target bit if and only if both control bits are in the logical state "1". In other words, if both control bits are "1", the target bit is flipped; otherwise, it remains unchanged.

4.1.2 Fredkin Gate

Edward Fredkin created the Fredkin gate, also known as the CSWAP gate and conservative logic gate, which is a computational circuit appropriate for reversible computing.
A Fredkin gate has a quantum cost of 5.

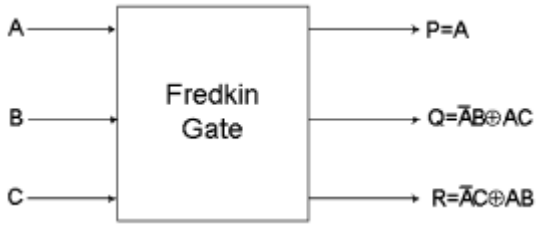

Fig -5: Fredkin Gate Circuit diagram

4.2 Full Adder circuit using Toffoli gates and Fredkin gate

The Full adder is designed with 4 Toffoli gates and 1 Fredkin gate. This is an example of leveraging reversible logic gates to construct efficient computational circuits. This approach focuses on maximizing computational accuracy while minimizing energy consumption, making it particularly suitable for applications demanding low-power implementations. Four Toffoli gates are strategically arranged to calculate the sum (S) output of the full adder. The Fredkin gate enables the full adder circuit to efficiently determine the carry-out bit based on the input bits and the sum output. The circuit is shown below.

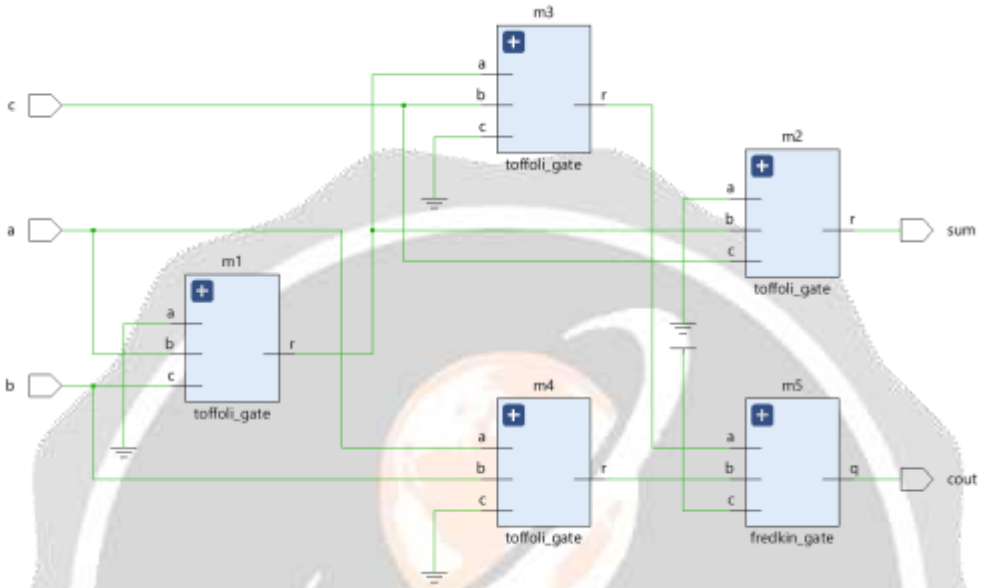

Fig -6: Schematic diagram of Full Adder using Toffoli gates and Fredkin gate

The simulation results for the Full adder using Toffoli gates and Fredkin gate is shown below.

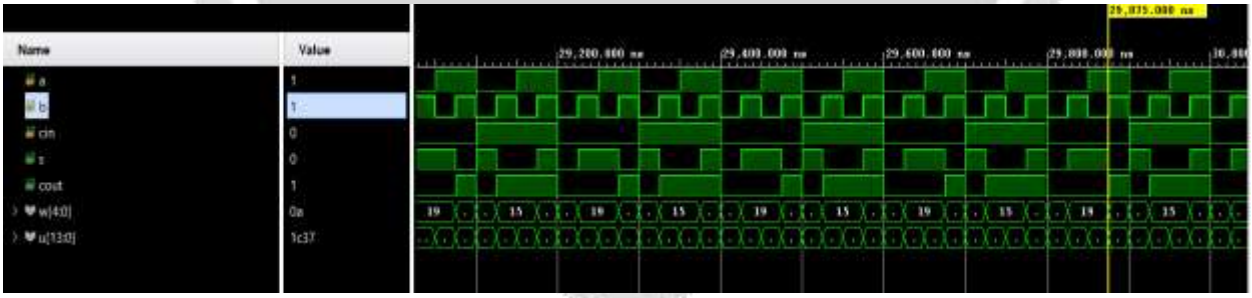

Fig -7: Simulation result of Full Adder

4.3 Multiplier using Toffoli gates and Modified Full adders

The design of Multiplier using Toffoli gates and Modified Full adder represents a systematic approach to constructing an energy-efficient and high-performance computational circuit capable of multiplying two binary numbers. This design harnesses the power of reversible logic gates and utilizes the previously designed full adders to achieve accurate multiplication while minimizing energy dissipation. Sixteen Toffoli gates are strategically arranged to perform the bitwise multiplication of the multiplicand and multiplier. These Toffoli gates operate on different combinations of multiplicand and multiplier bits to generate partial product bits, representing the intermediate multiplication results. Three full adders, previously designed using Toffoli and Fredkin gates, are employed to accumulate the partial products and generate the final product of multiplication. The output bits of the

Toffoli gates representing partial products are fed into the full adders, which perform binary addition while considering the carry bits to accumulate the multiplication results.

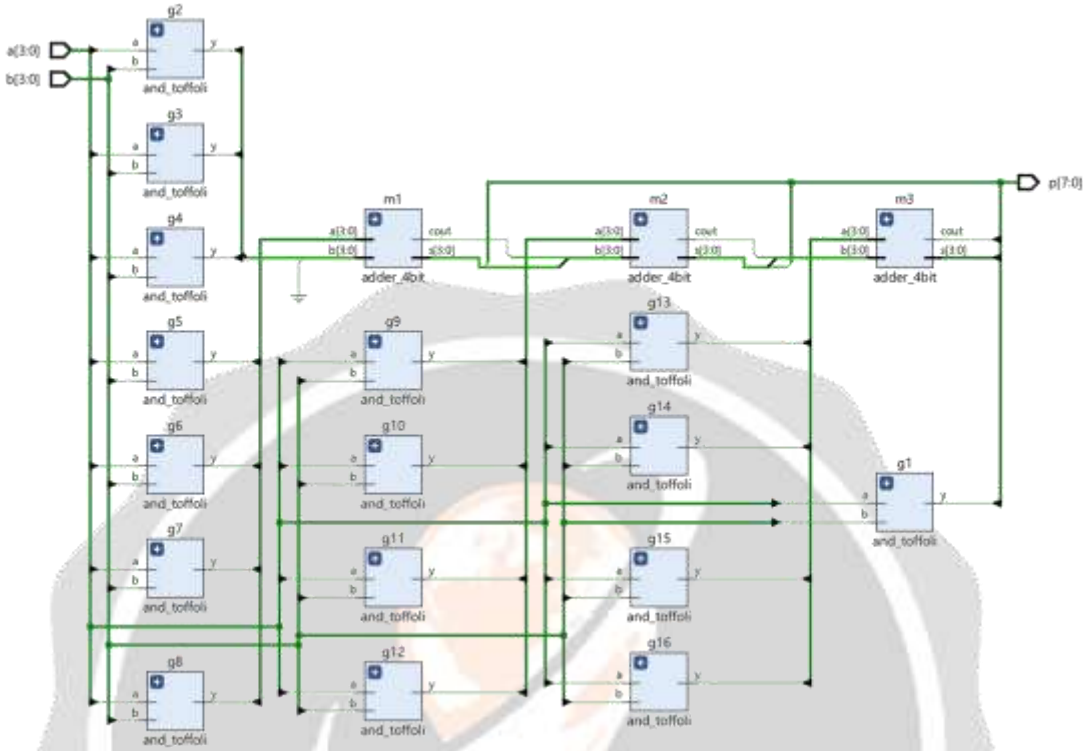

Fig -8: Schematic diagram of Multiplier using Toffoli gates and Modified Full adder

The simulation results for the above Multiplier is shown below.

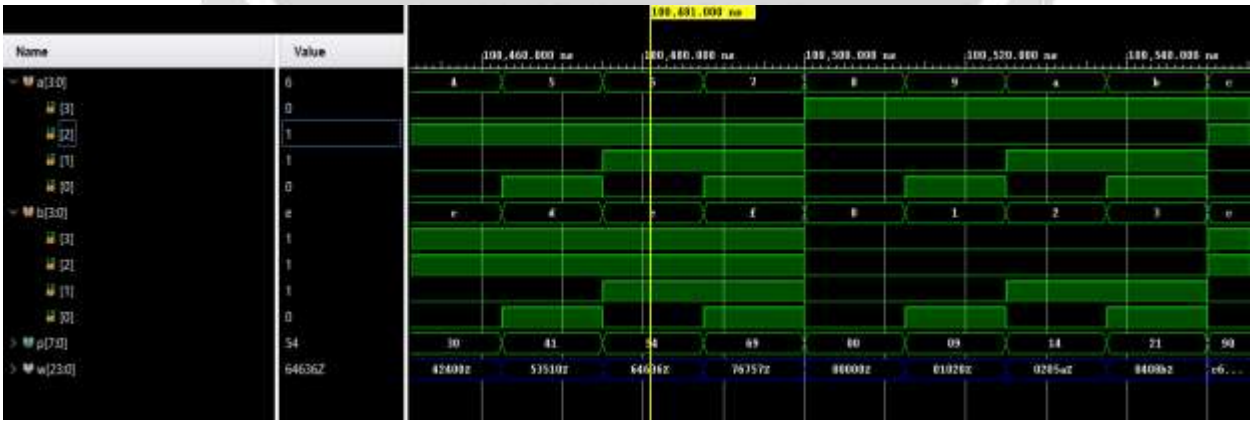

Fig -9: Simulation result of proposed multiplier

5. RESULT AND DISCUSSION

The Power report for the designed multiplier is shown below**.**

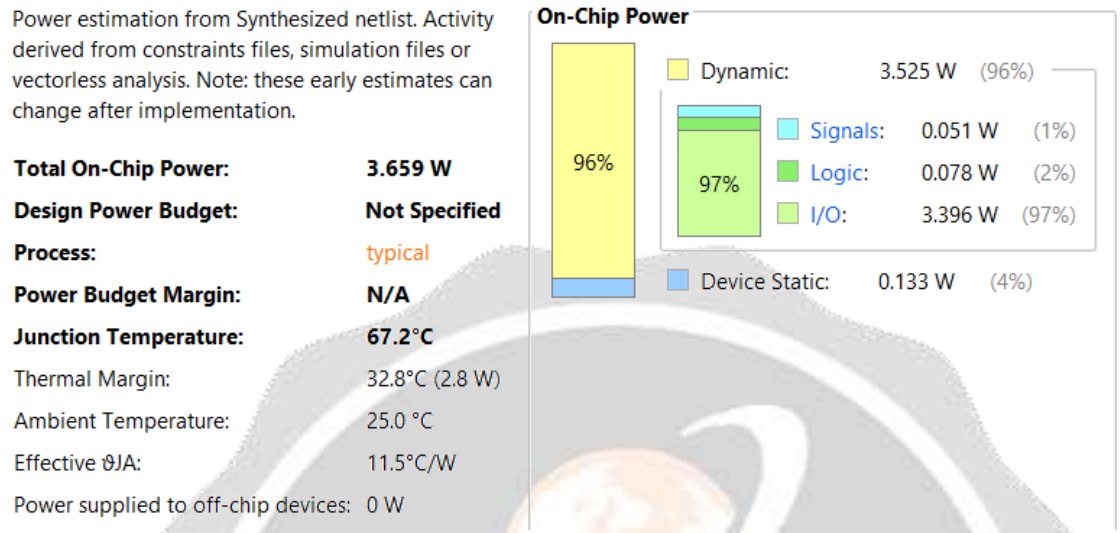

Fig -10: Power report of the proposed multiplier

Name 1	Slice LUTs (17600)	F7 Muxes (8800)	F8 Muxes (4400)	Bonded IOB (54)
N mul_4bit	21	6	3	16

Comparison Table

Table -2: Comparison of parameters between existing system and proposed system

System	Gates used	Number of gates	No. of MFA	Number of constant inputs	Number of Garbage outputs	Power Dissipation
Existing System	Peres Gates	40	12	28	32	4.13W
Proposed System	Toffoli Gates	28	3	28	32	3.659W

6. CONCLUSION

This Multiplier represents a strategic balance between computational efficiency, energy conservation, and circuit complexity. Multiplier is basic arithmetic cell in computer arithmetic units. The multiplier is designed by using Toffoli gates. By leveraging the reversible properties of Toffoli gates and the accumulative capabilities of full adders, this design offers a viable solution for implementing efficient binary multiplication operations. The power consumption can be reduced by reducing the garbage outputs. Hence, we can say that the proposed Multiplier is better than existing one. Optimization and refinement of the multiplier design, along with advancements in reversible logic techniques and technology scaling, hold promise for enhancing the efficiency and scalability of reversible multiplier circuits in future computing systems.

7. REFERENCES

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